

FIG.1

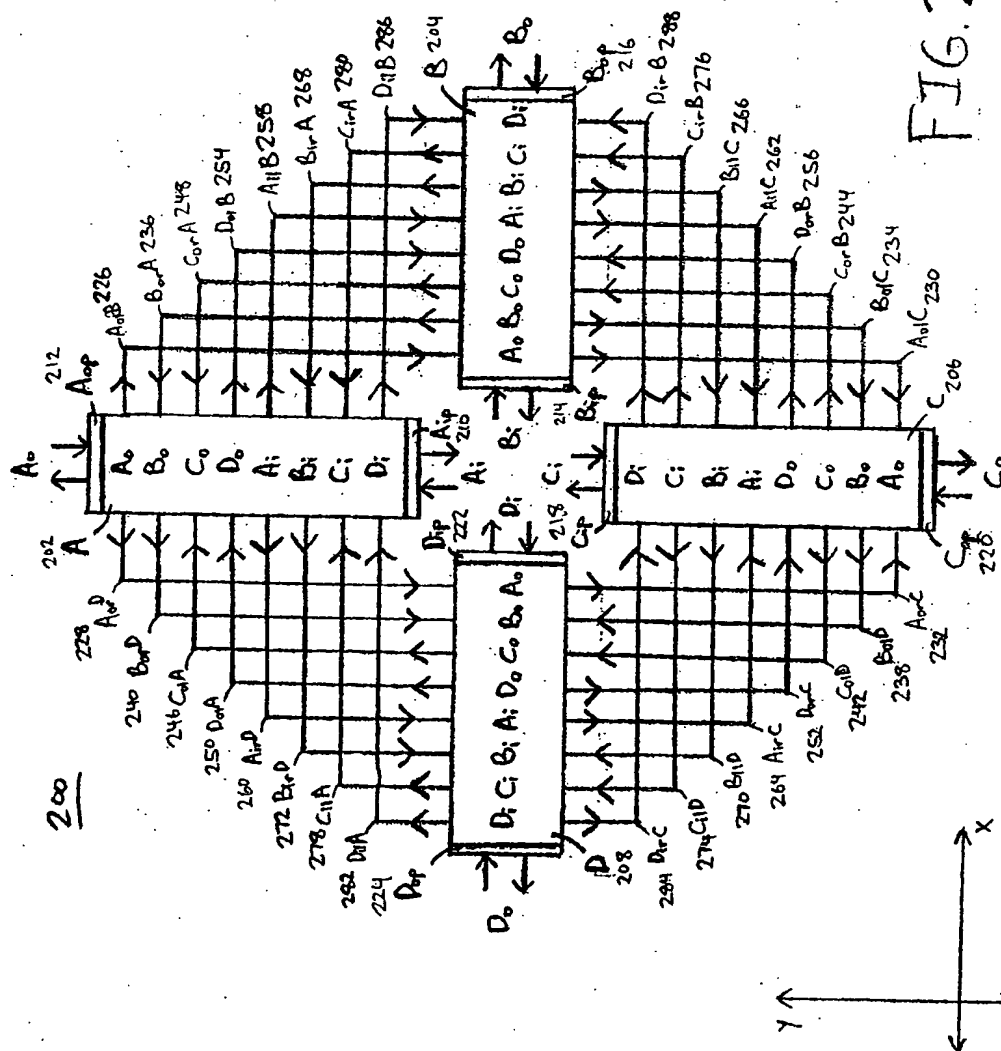


FIG. 2

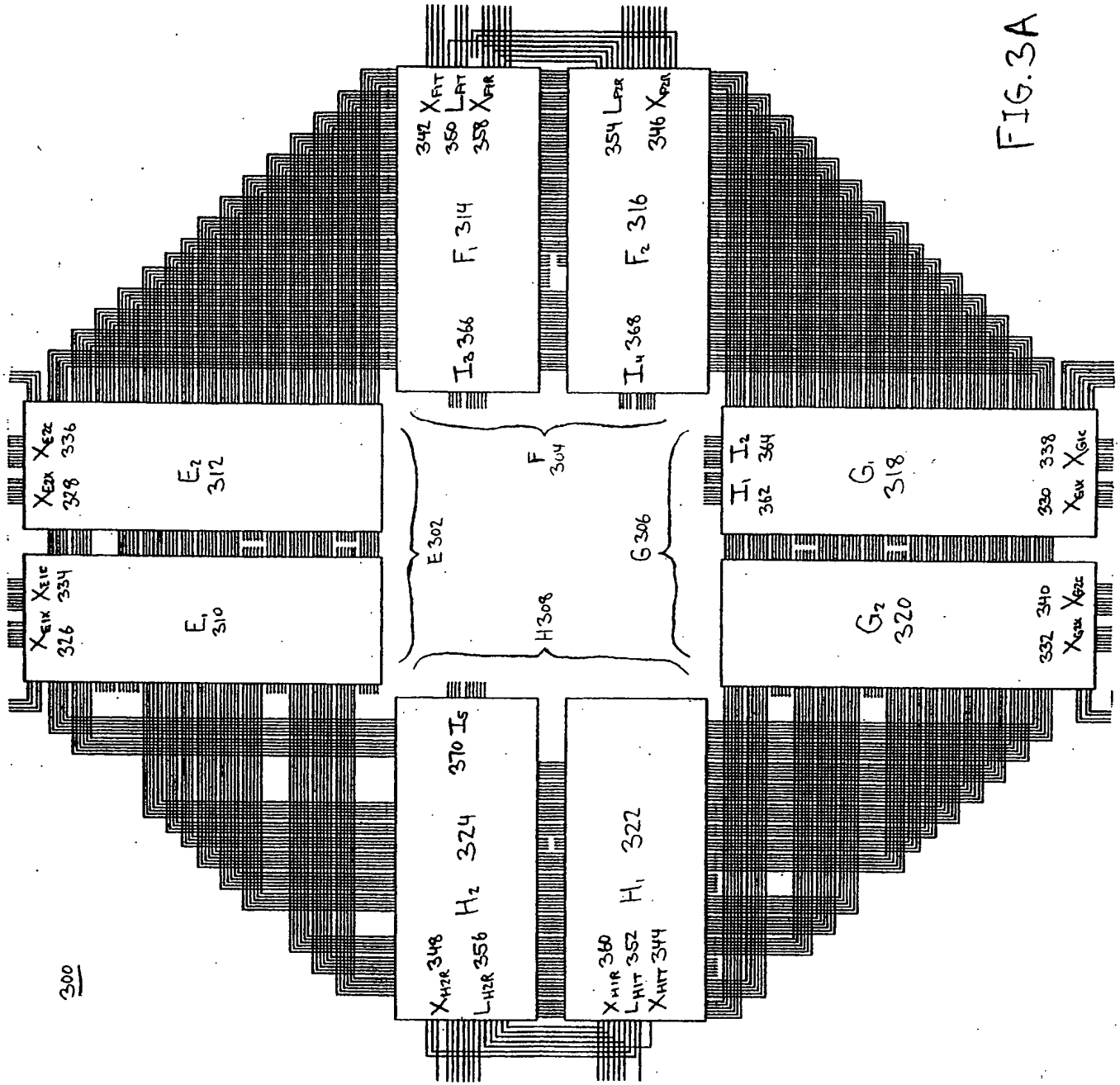


FIG. 3A

315



FIG. 3B

385

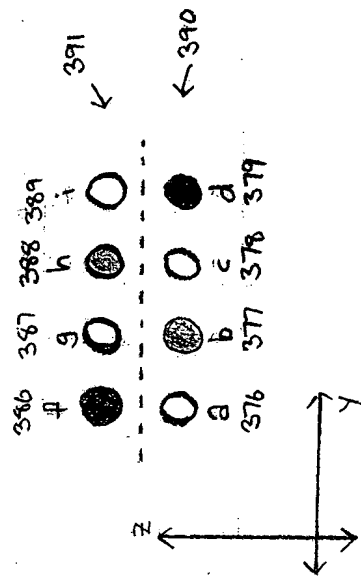


FIG. 3C

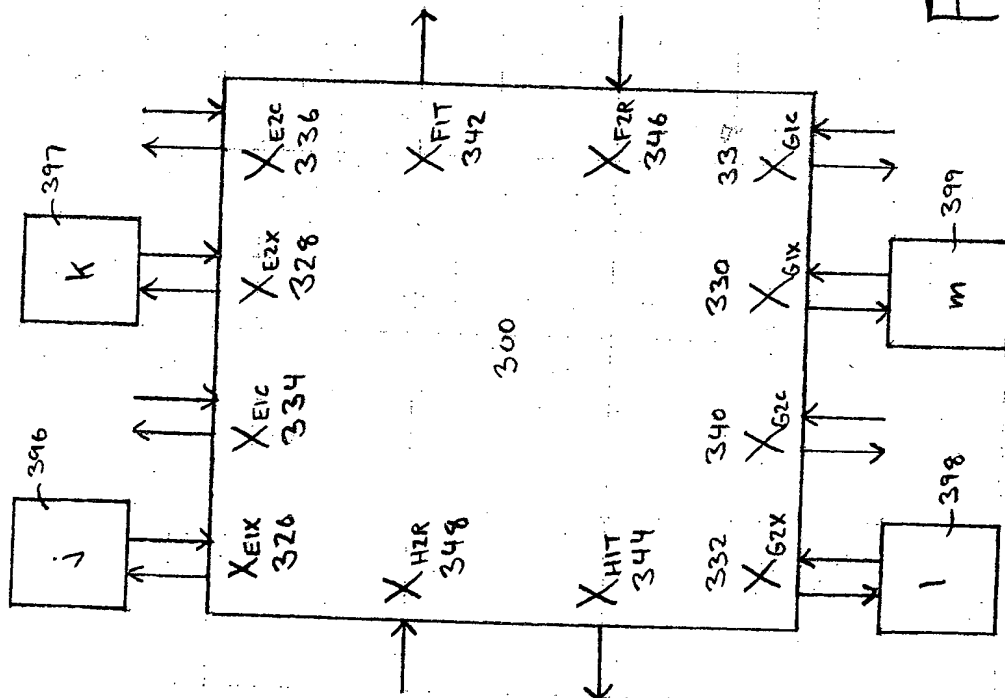


FIG. 3D

FIG. 4

TABLE 400

XAUI Protocol		
Received From Out of Bus	Communicated Within Bus	Transmitted to Out of Bus
40 data bits	40 data bits	80 data bits
4 link bits	4 link bits	
4 lock bits	4 lock bits	
4 clock bits	4 clock bits	4 clock bits
4 fast clock bits	4 fast clock bits	
1 CLOCK MODE SELECT bit	1 CLOCK MODE SELECT bit	

CDL Protocol		
Received From Out of Bus	Communicated Within Bus	Transmitted to Out of Bus
40 data bits	40 data bits	80 data bits
4 link bits	4 link bits	4 link bits
4 lock bits	4 lock bits	4 lock bits
4 clock bits	4 clock bits	4 clock bits
4 fast clock bits	4 fast clock bits	
1 CLOCK MODE SELECT bit	1 CLOCK MODE SELECT bit	

XGMII Protocol		
Received From Out of Bus	Communicated Within Bus	Transmitted to Out of Bus
40 data bits	80 data bits	40 data bits
4 lock bits	4 lock bits	
4 clock bits	4 clock bits	4 clock bits
3 MODE SELECT bits		
1 DIFFERENTIAL CLOCK MODE SELECT bit		
	1 CLOCK MODE SELECT bit	
		4 output enable bits

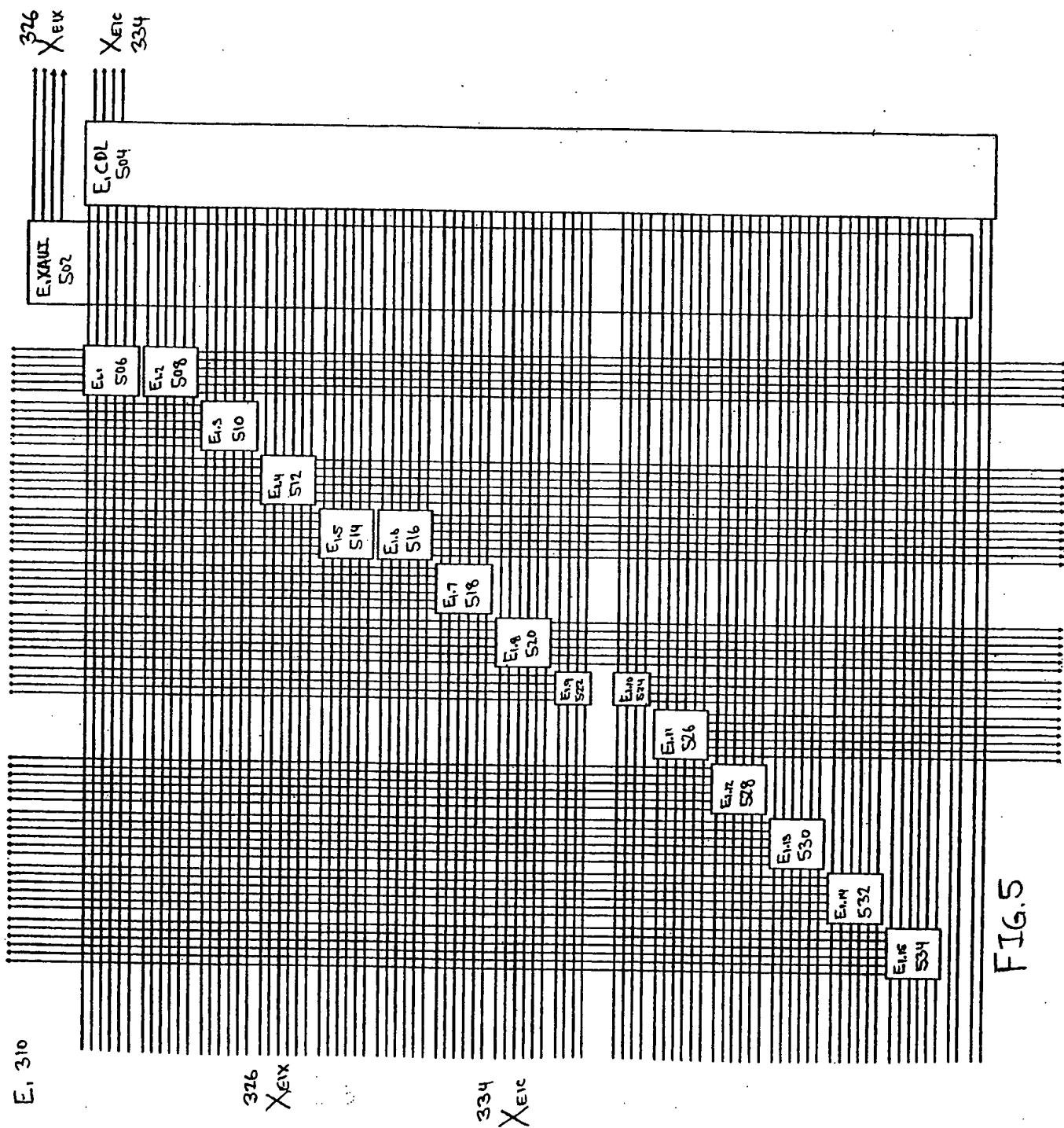


FIG. 5

FIG. 6

E_{1.1} 506

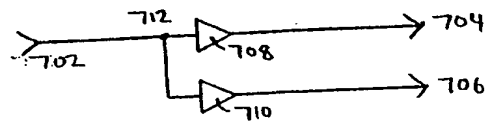


FIG. 7

E_{1.4} 516

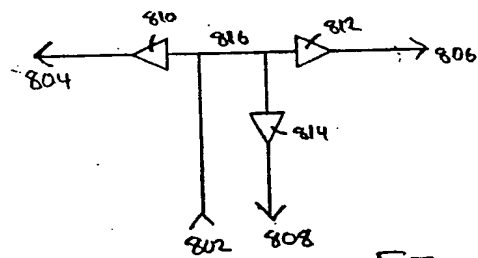


FIG. 8

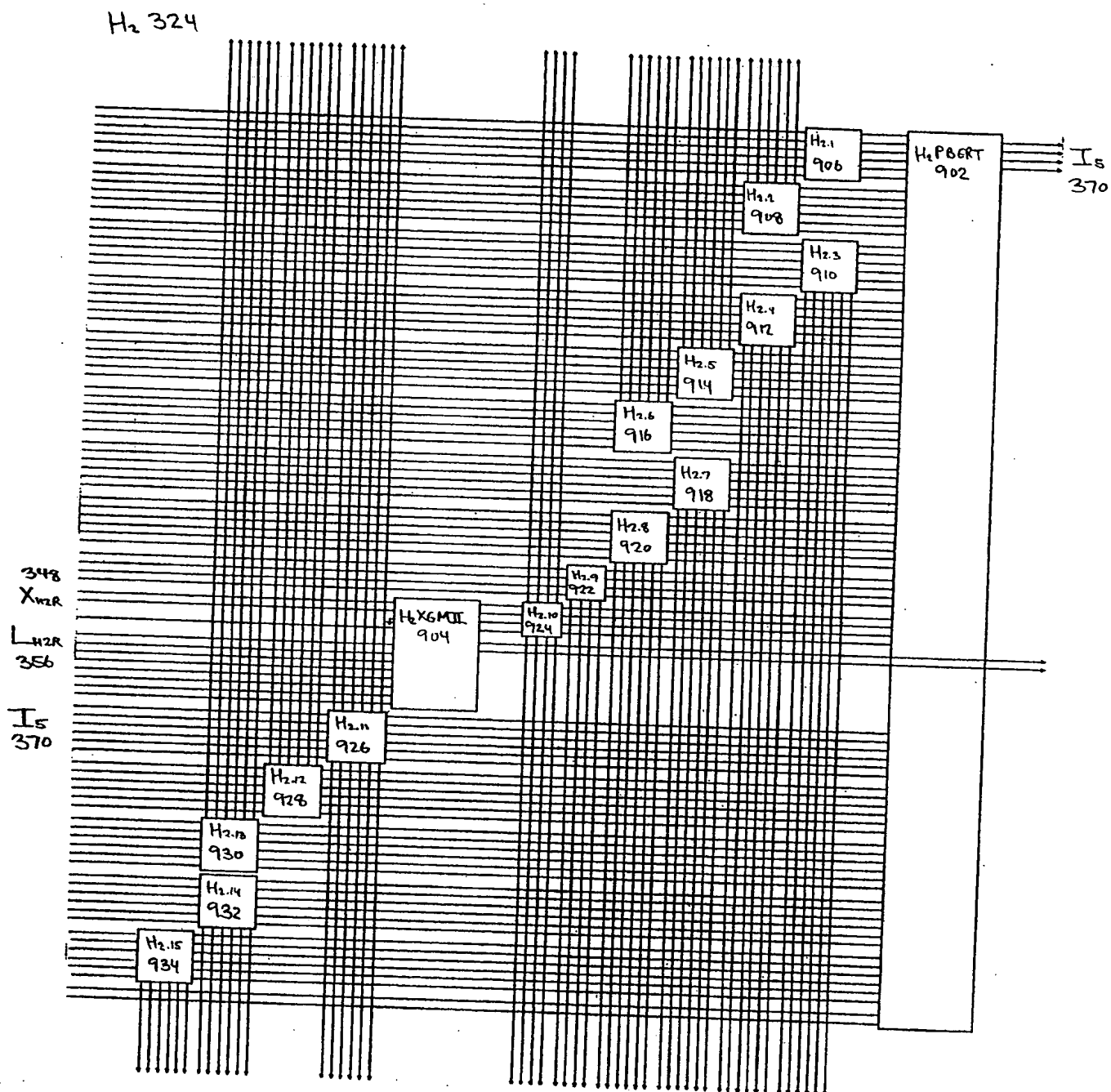
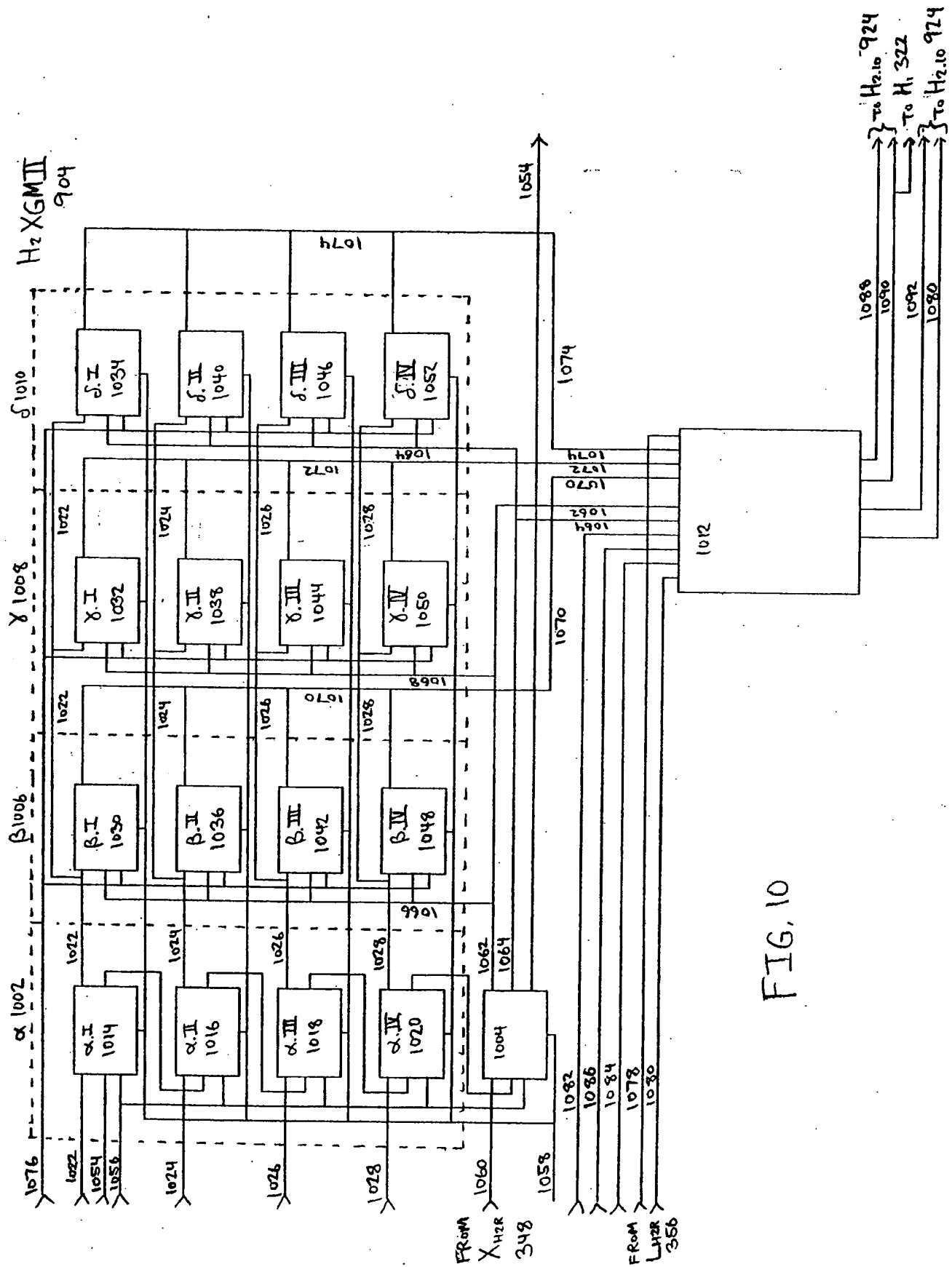


FIG. 9



$\alpha.I.1014$

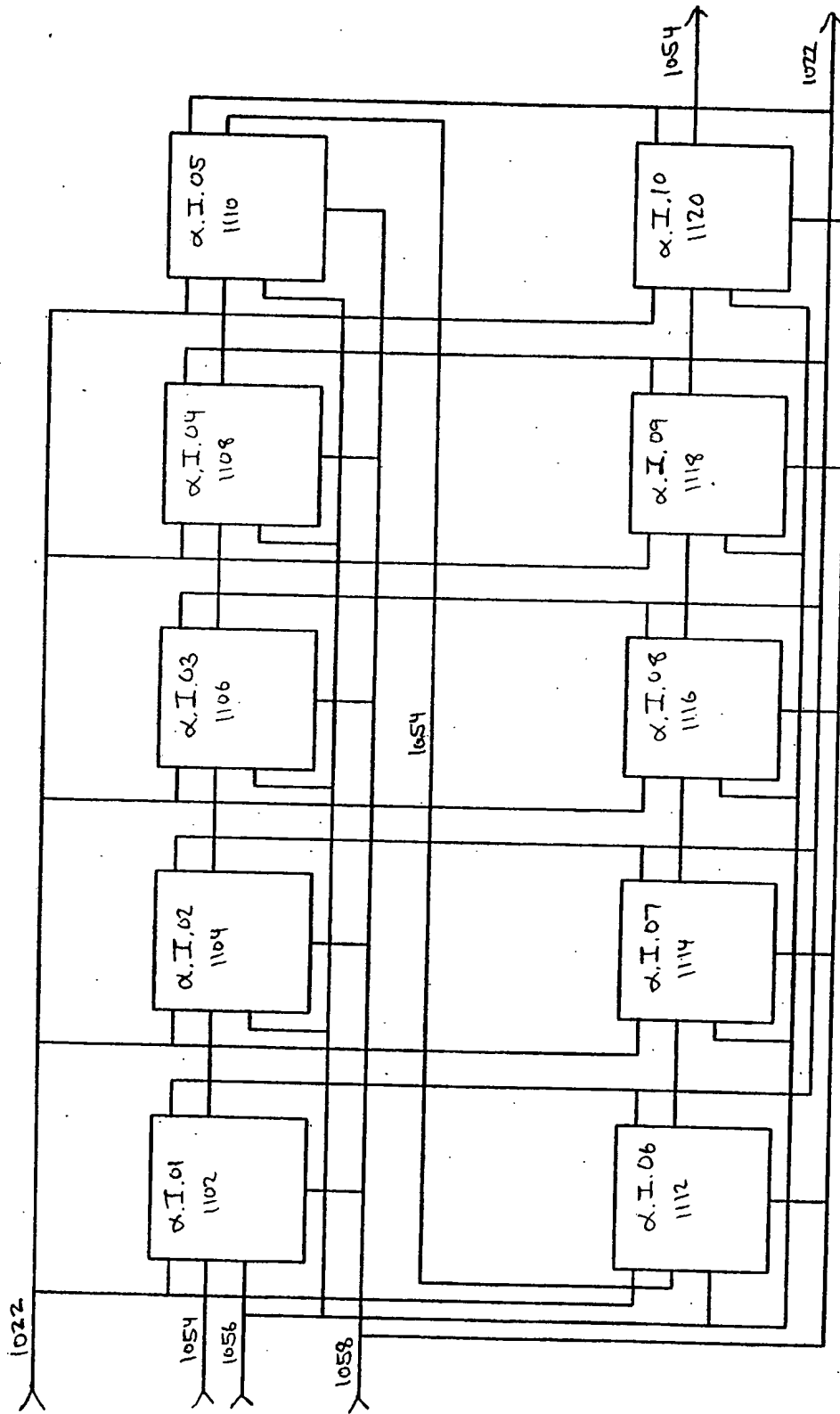


FIG. 11

TRANSMITTER CLOCK PHASE DELAY CIRCUIT 1004

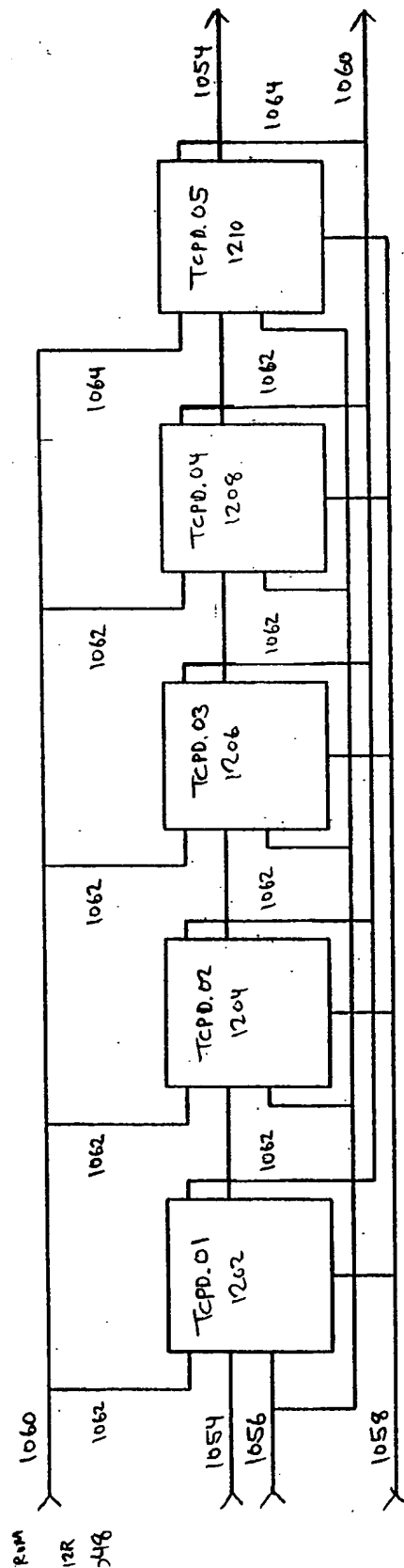


FIG. 12

$\alpha.I.01.1102$

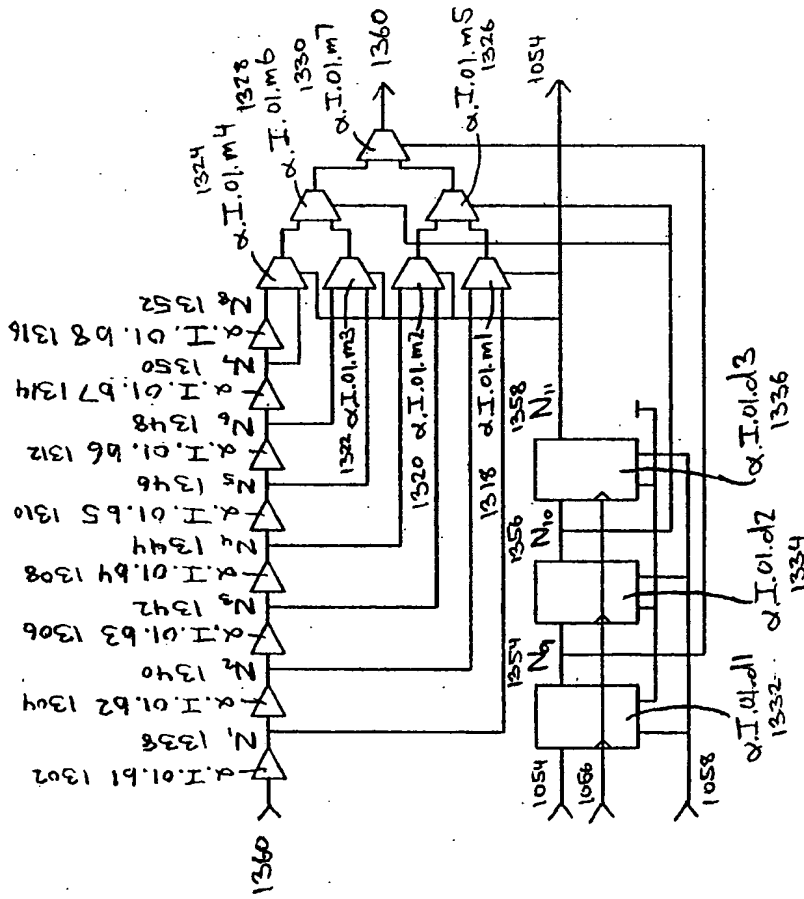


FIG. 13A

FIG. 13B

N_9	N_{10}	N_{11}	Output
0	0	0	N_1
0	0	1	N_2
0	1	0	N_3
0	1	1	N_4
1	0	0	N_5
1	0	1	N_6
1	1	0	N_7
1	1	1	N_8

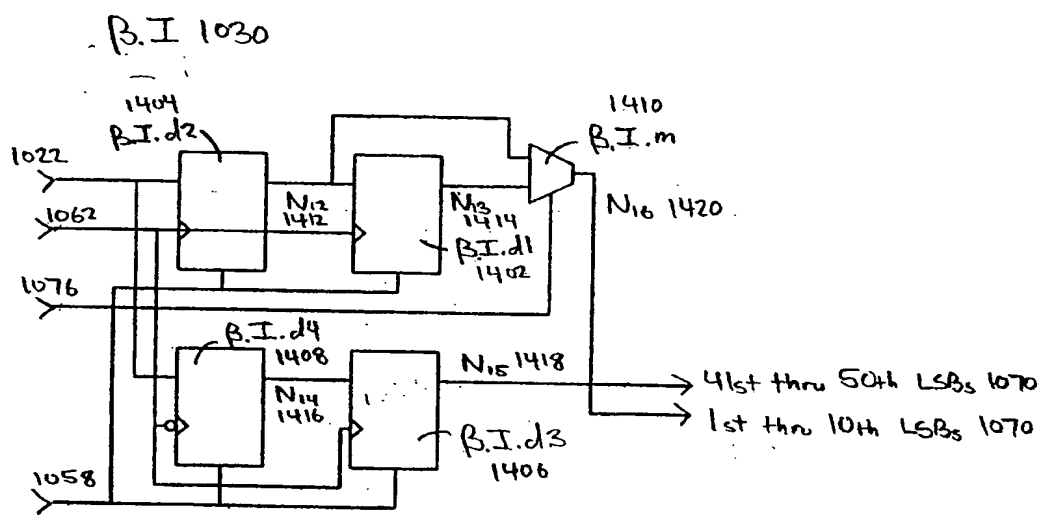
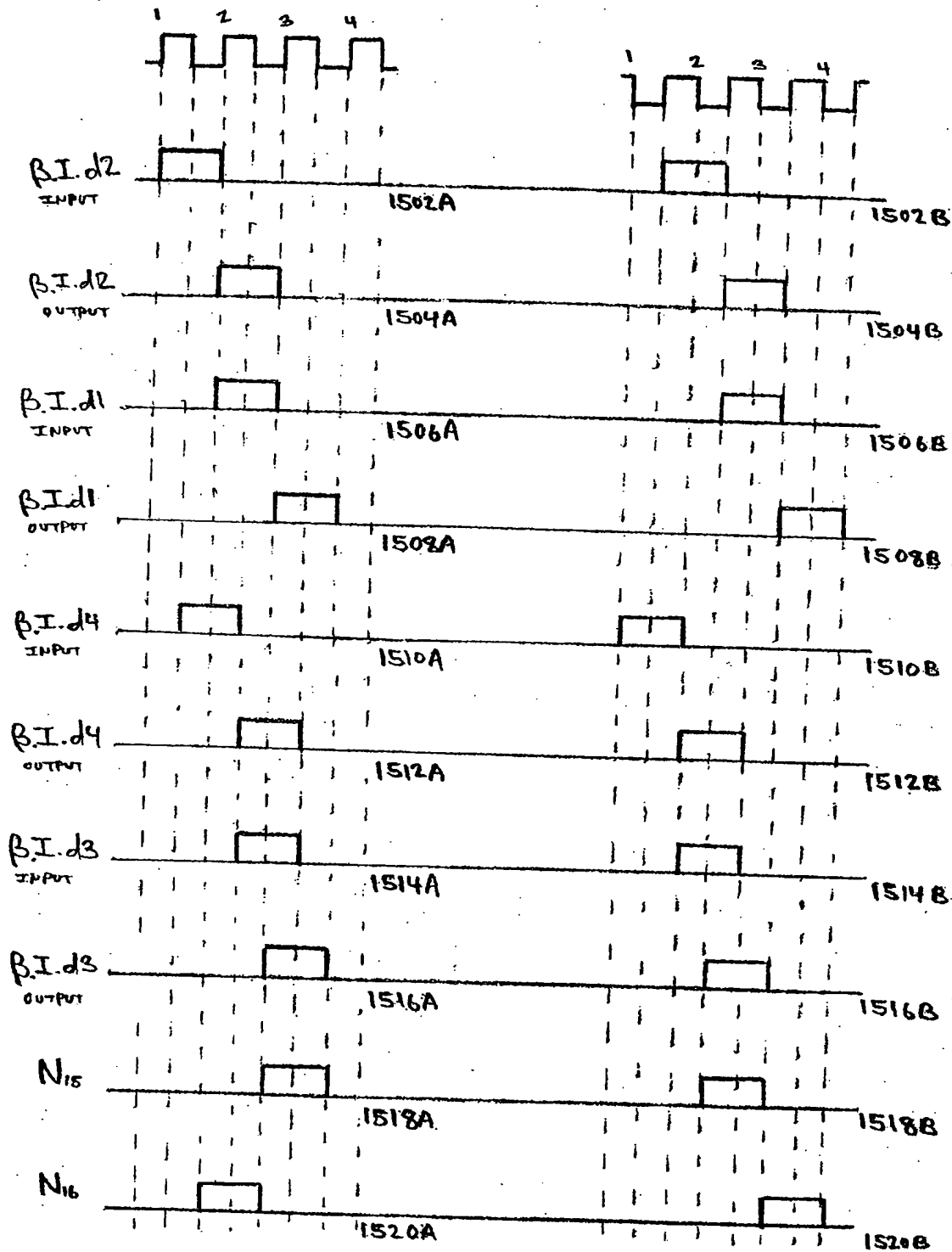


FIG. 14

FIG. 15A
1500A

FIG. 15B
1500B



TRANSMITTER REGISTER MULTIPLEXER 1012

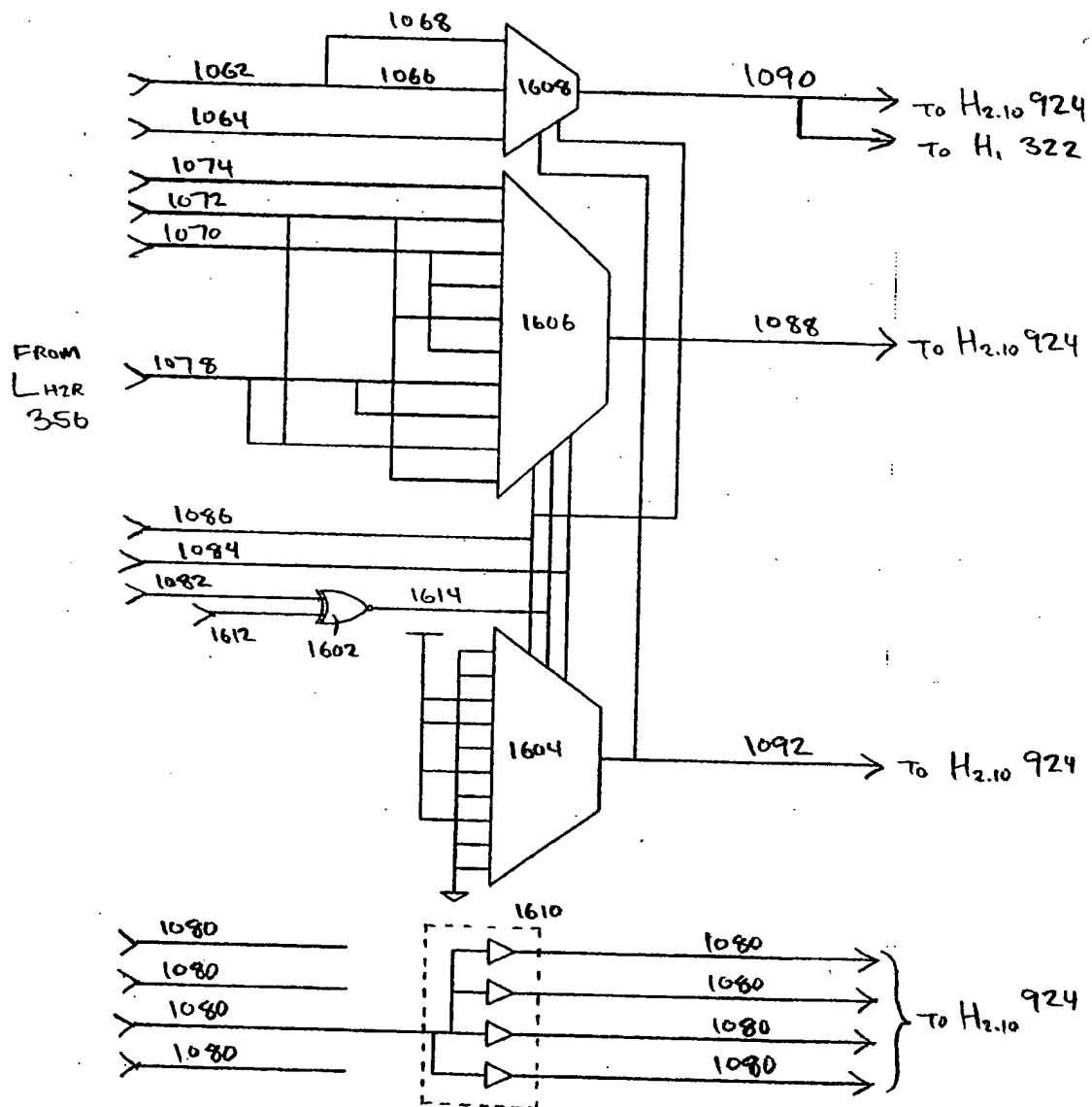
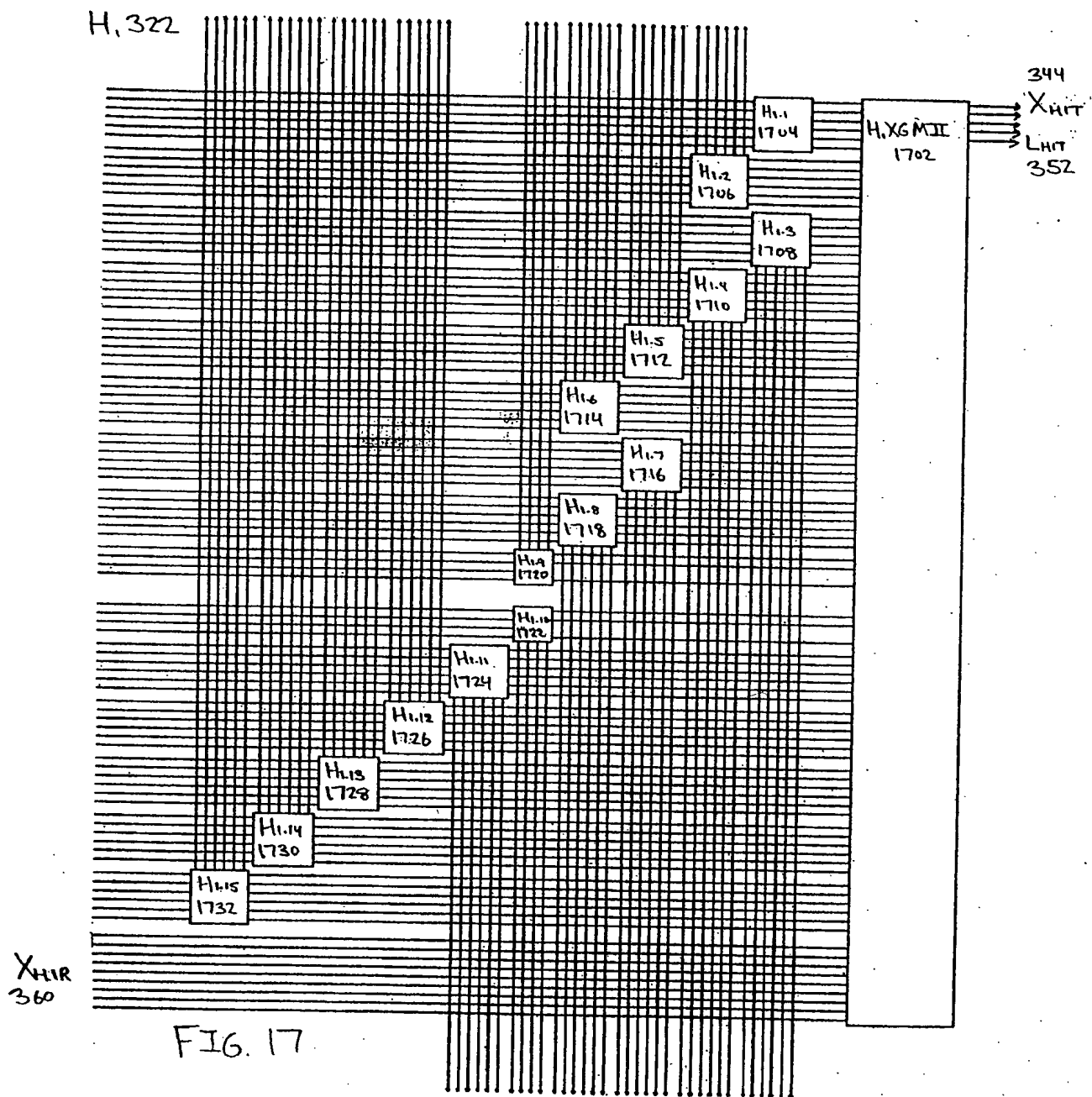


FIG. 16



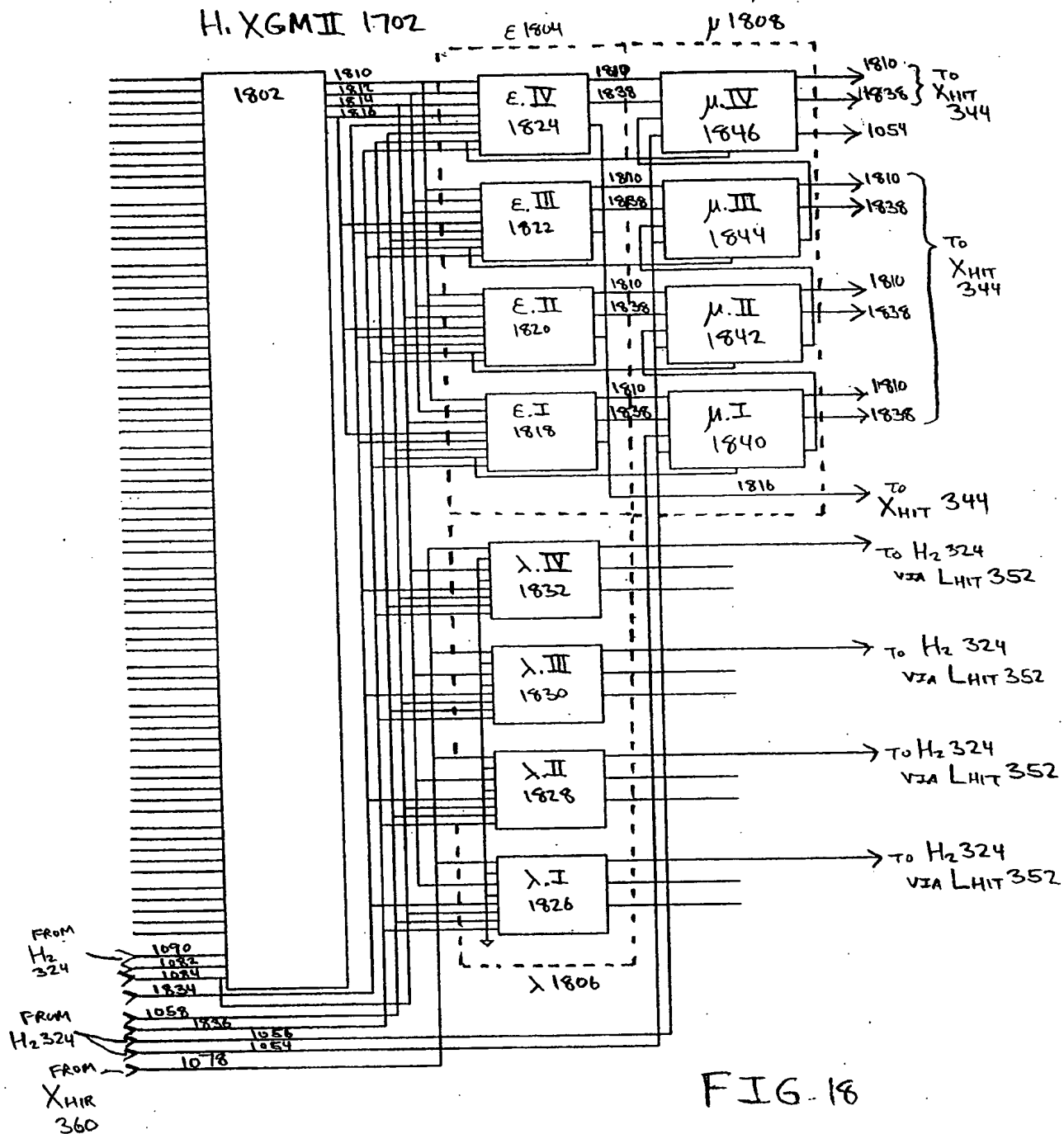


FIG-18

RECEIVER AND MULTIPLEXER 1802

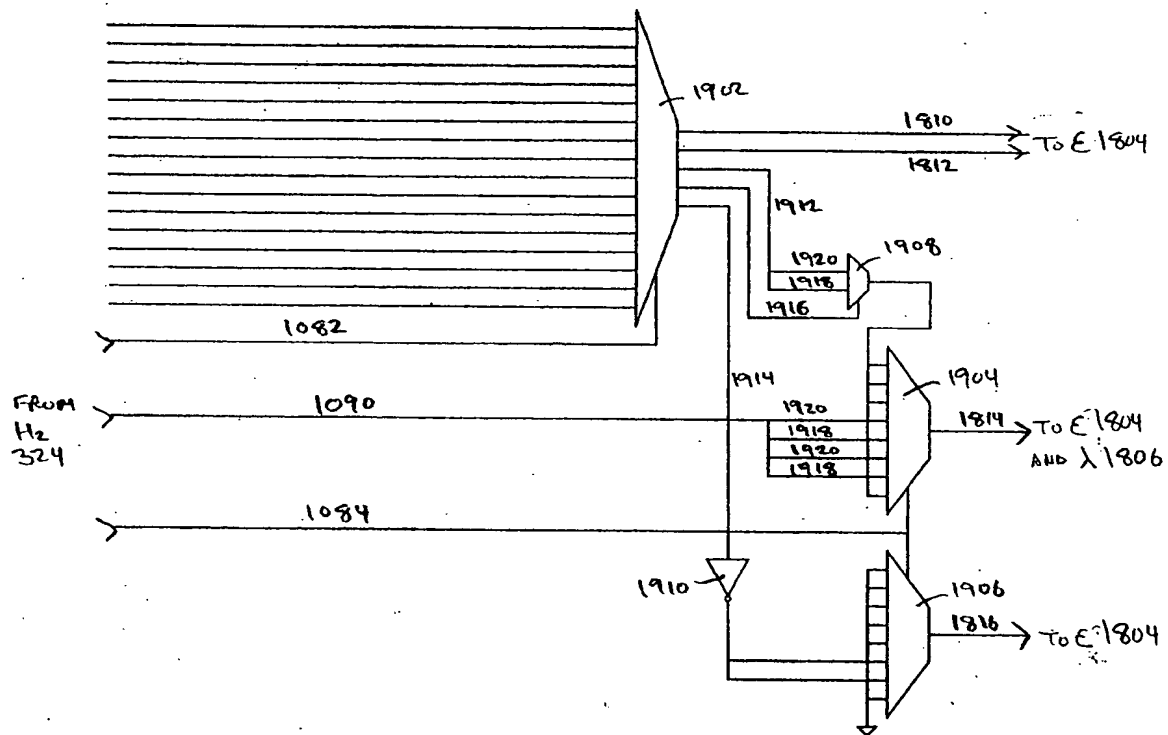


FIG. 19

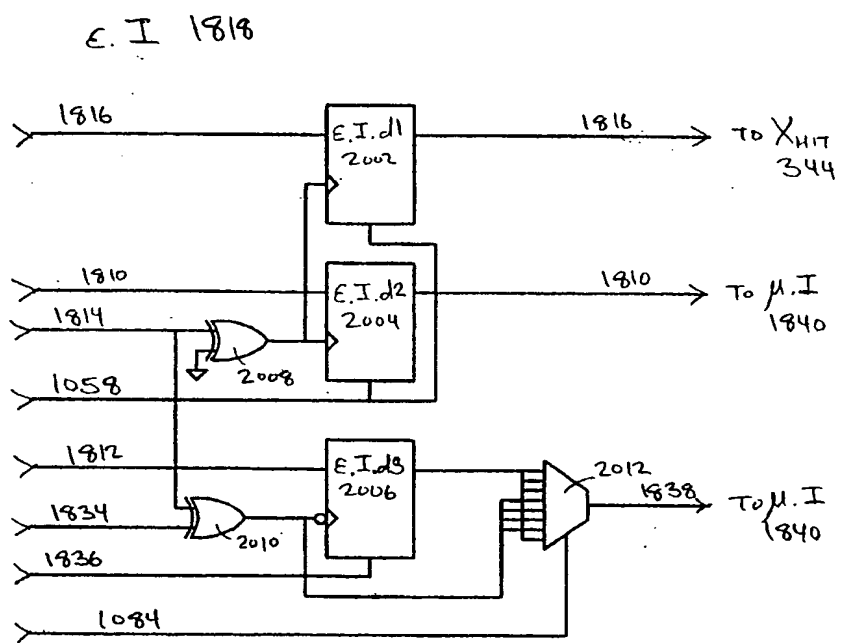
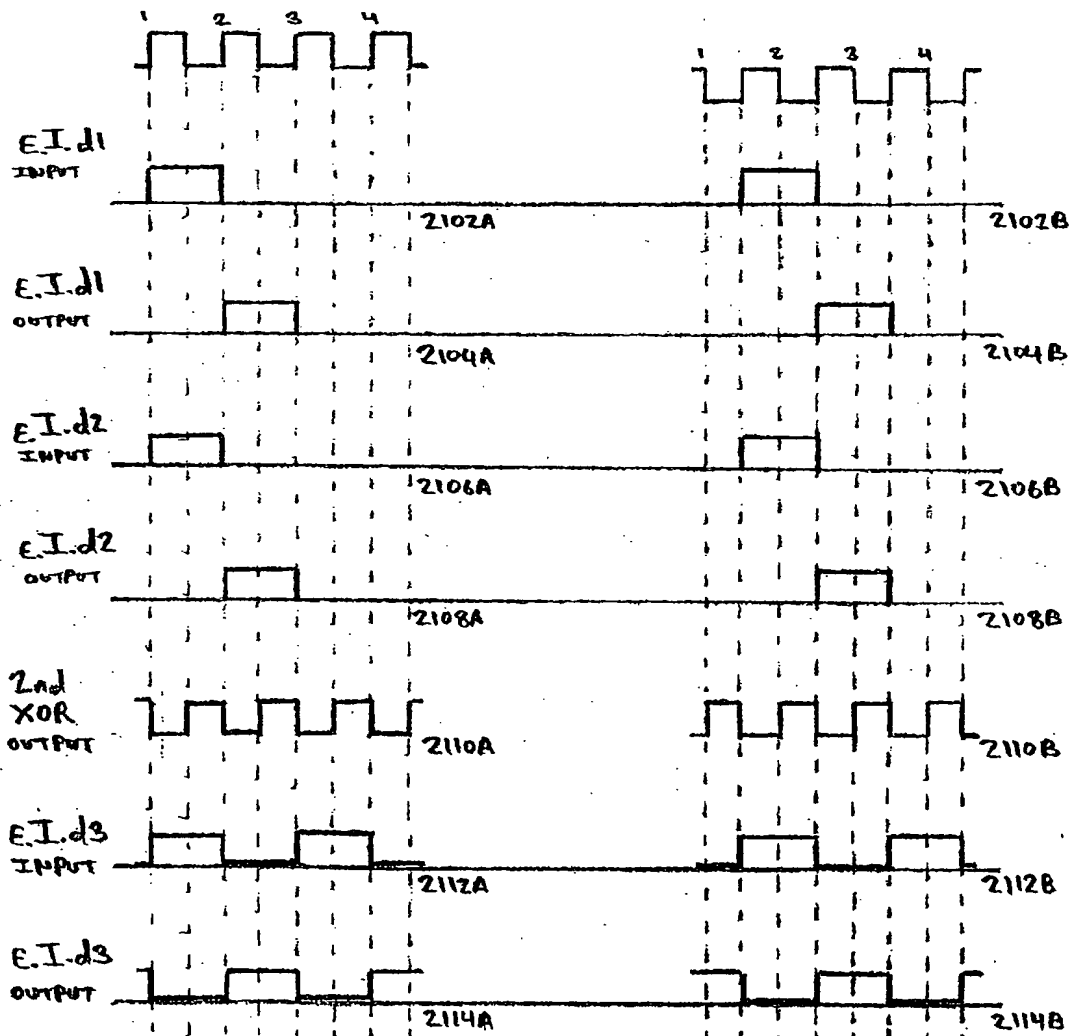


FIG. 20

FIG. 21A
2100A

FIG. 21B
2100B



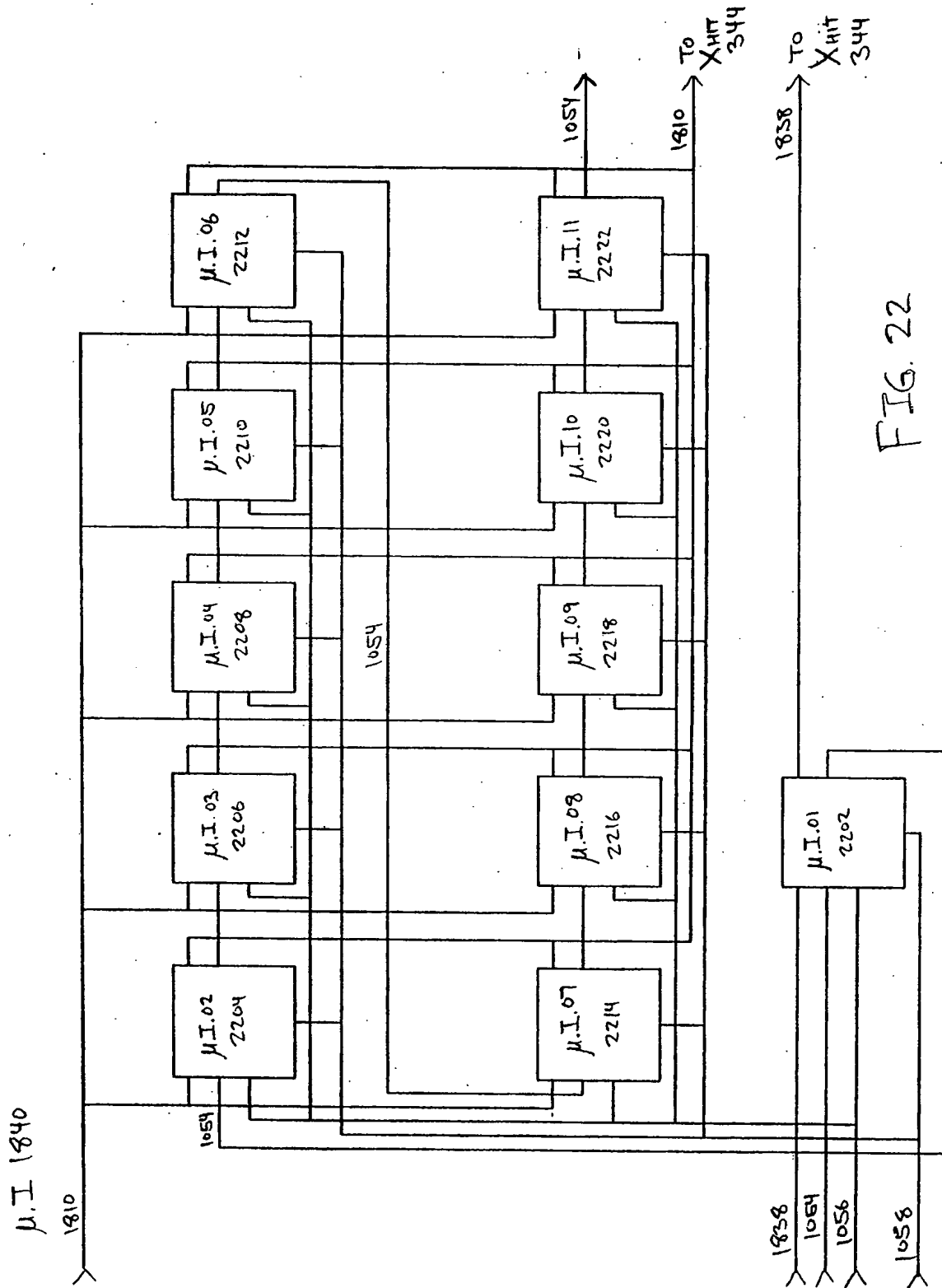


FIG. 23

2300

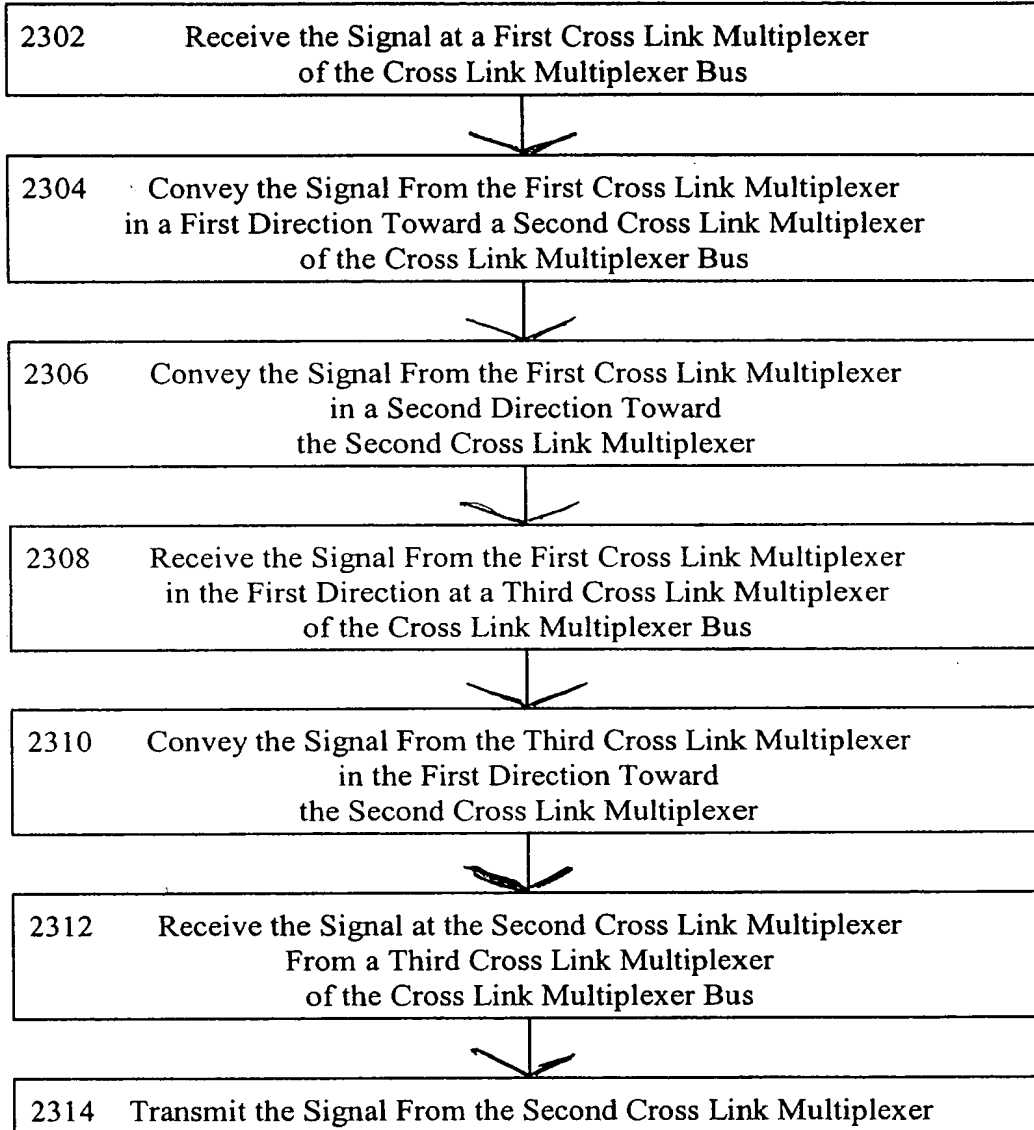


FIG. 24

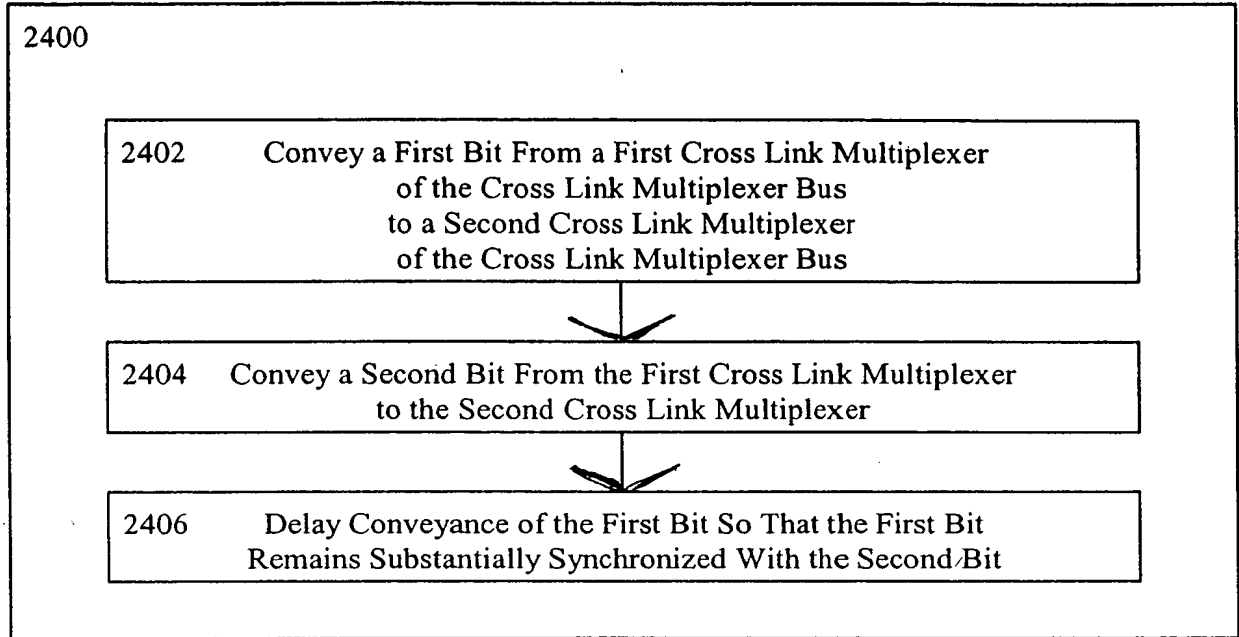


FIG. 25

2500

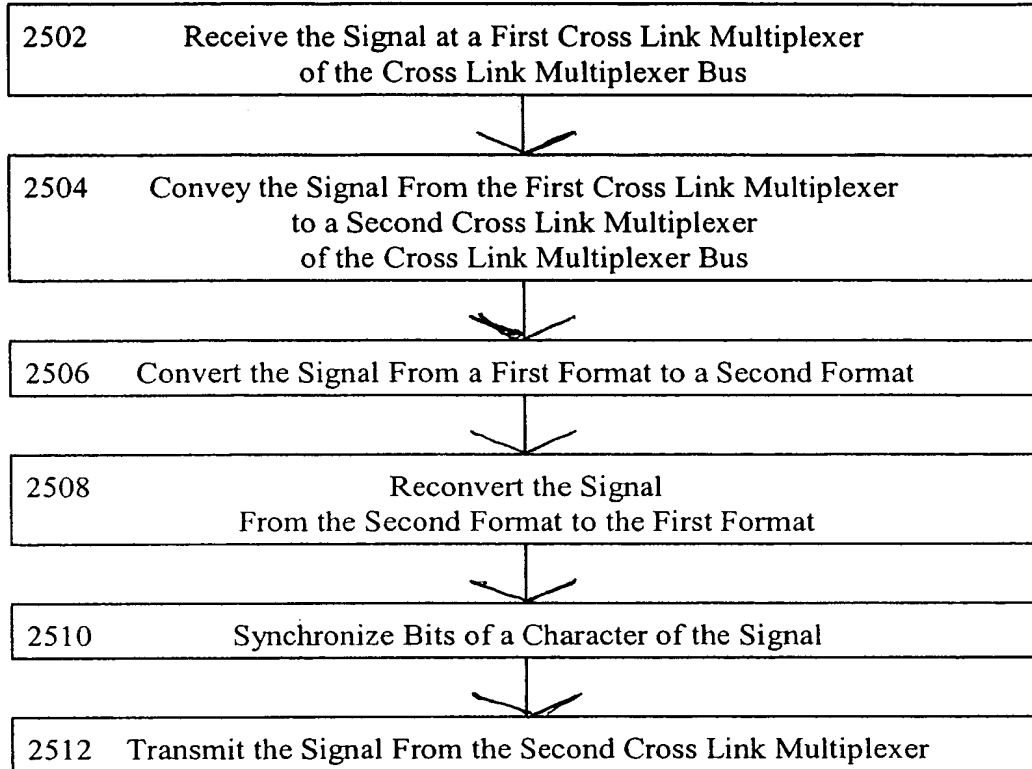


FIG. 26

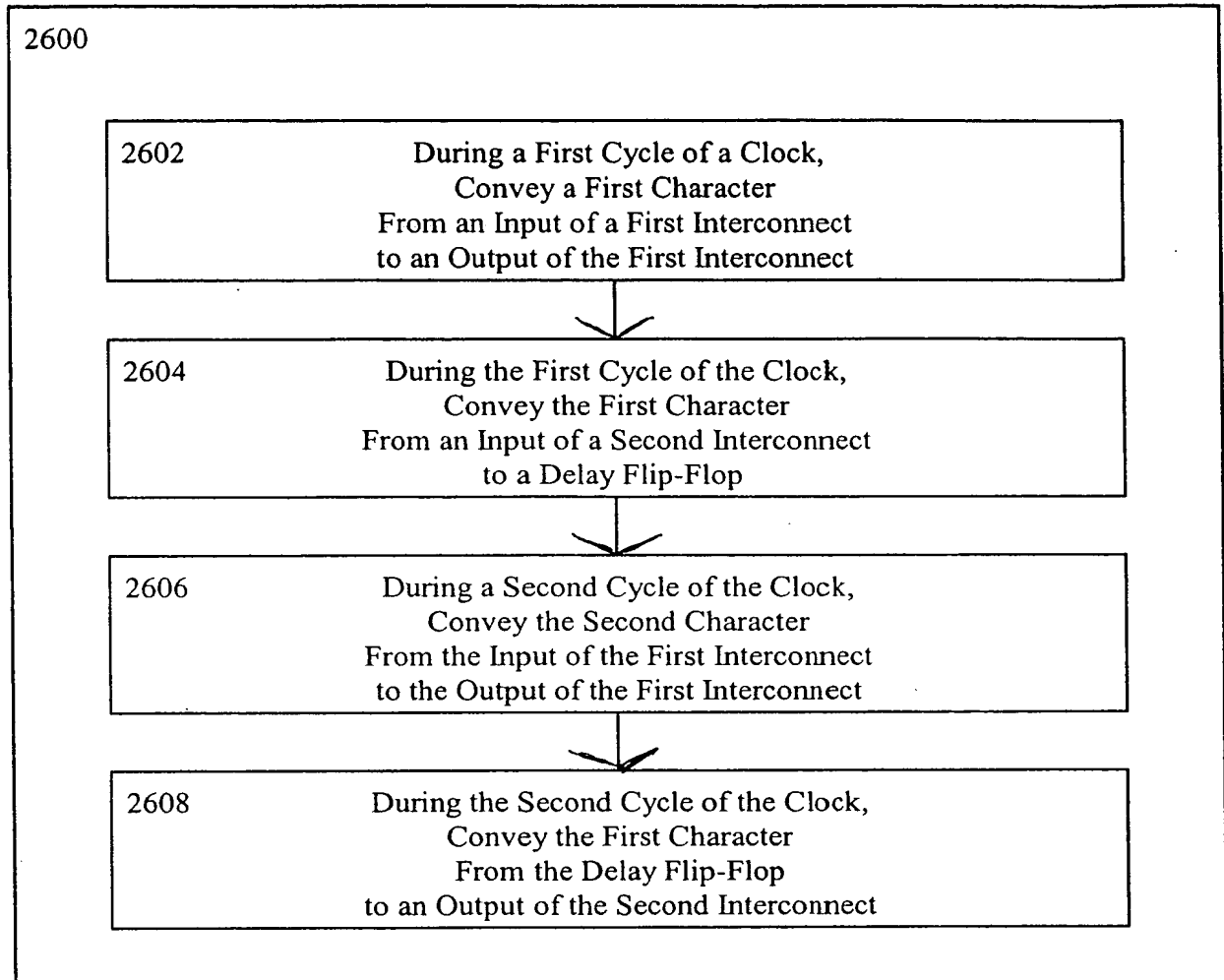


FIG. 27

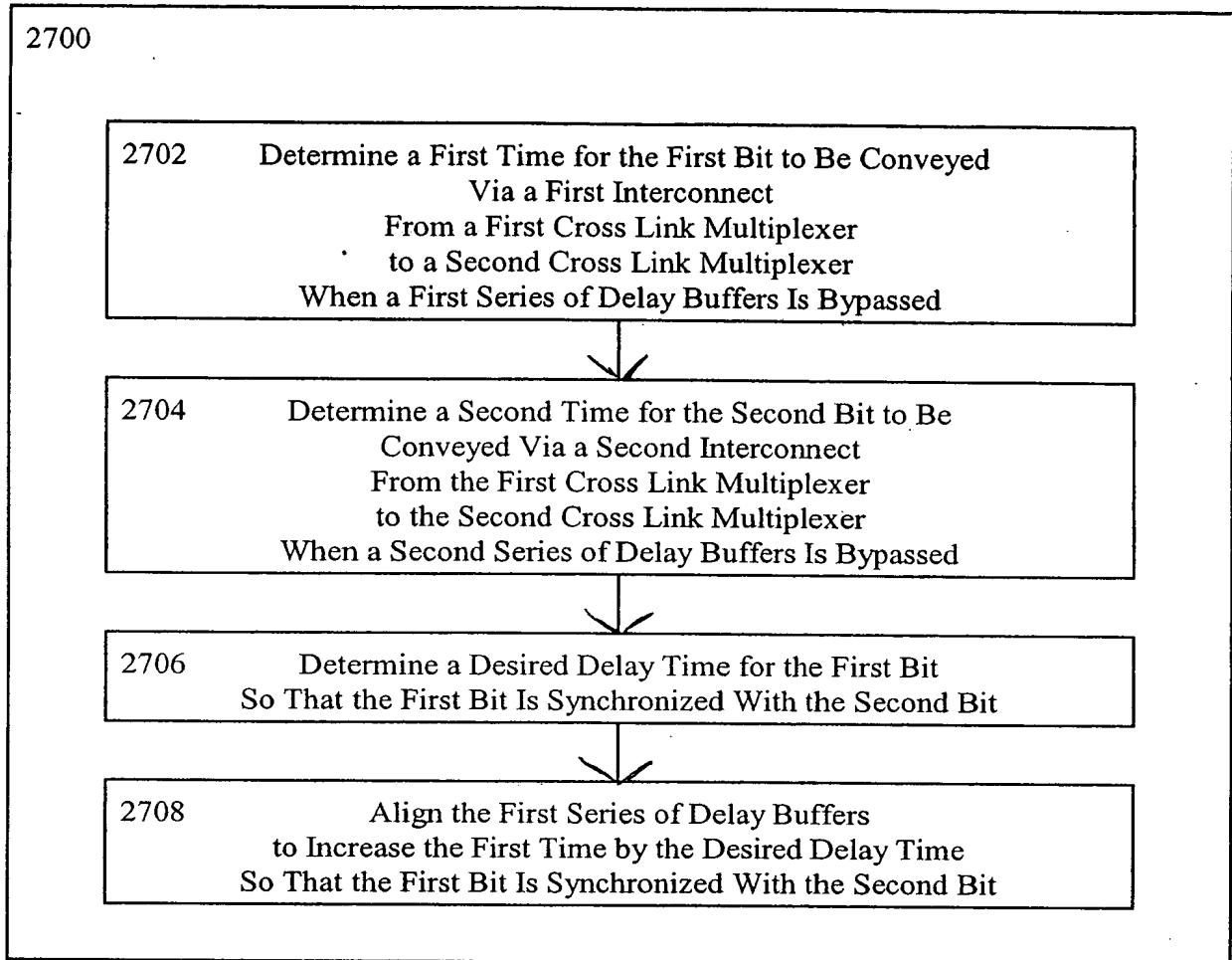


FIG. 28

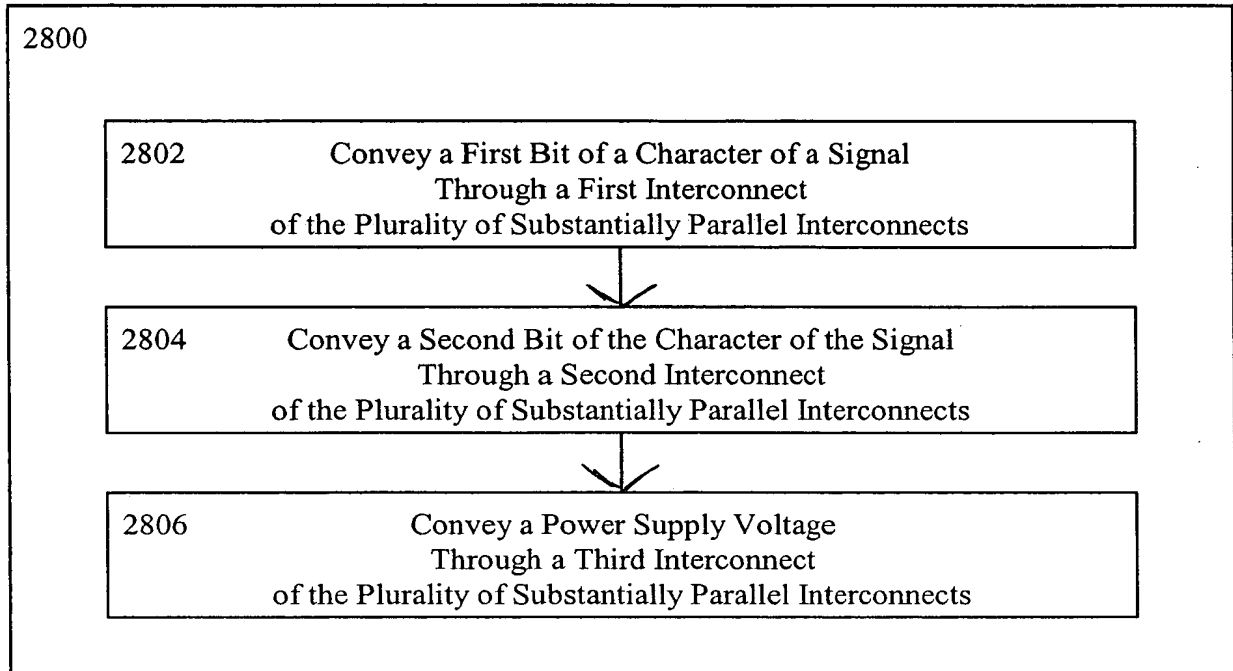


FIG. 29

